19-4477; Rev 0; 2/09

EVALUATION KIT AVAILABLE

Quad, High-Voltage EL Lamp Driver with I²C Interface

MAX14521E

General Description

The MAX14521E is a quad-output high-voltage DC-AC converter that drives four electroluminescent (EL) lamps. The device features a 2.7V to 5.5V input range that allows the device to accept a variety of voltage sources such as single-cell lithium-ion (Li+) batteries. The lamp outputs of the device generate up to 300V_{P-P} for maximum lamp brightness. The high-voltage outputs are ESD protected up to ±15kV Human Body Model (HBM), ±6kV Contact Discharge, and ±8kV Air Gap Discharge, as specified in IEC 61000-4-2.

The MAX14521E uses a high-voltage full-bridge output stage to convert the high voltage generated by the boost converter to a sinusoidal output waveform. The MAX14521E utilizes a high-frequency spread-spectrum oscillator to reduce the amount of EMI/EFI generated by the boost-converter circuit.

The MAX14521E provides an I²C interface to set the boost converter and EL output switching frequencies through an 8-bit register and the peak output voltages with 5 bits of resolution. The MAX14521E also provides an adjustable automatic ramping feature that slowly increases or decreases the peak output voltage when a change is made to the output amplitude. The slew rate of the automatic ramp is set with 3 bits of resolution through the I²C interface and it is independent for each channel. The MAX14521E features an audio auxiliary input AUX that modulates the EL output voltage and frequency for dynamic lighting effects.

The MAX14521E is available in a small, 4mm x 4mm, 24-pin TQFN package, and specified over the extended -40°C to +85°C operating temperature range.

Applications

Keypad Backlighting

LCD Backlighting

PDAs

Smartphones

Automotive Instruments Clusters

Pin Configuration appears on last page

Features

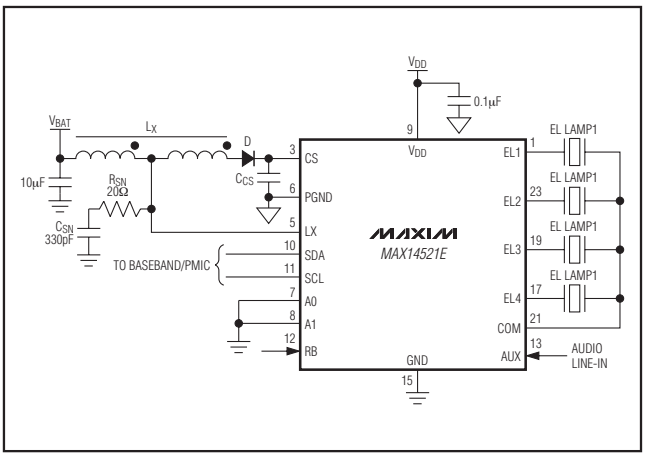
- **300V_{P-P} Maximum Output for Highest Brightness**
- **ESD-Protected EL Lamp Outputs**
  - **±15kV Human Body Model**
  - **±6kV IEC 61000-4-2 Contact ESD Protection**
  - **±8kV IEC 61000-4-2 Air Gap Discharge**
- **2.7V to 5.5V Input Voltage Range**
- **I²C Interface for Control of Brightness, EL Frequency, Boost Frequency, Shape**
- **Sinusoidal Output for Low Audible Noise**
- **Individual Dimming Control**
- **Individually Adjustable Output Brightness Ramping Rate**
- **±3% EL Output Frequency Accuracy for Truest EL Panel Color**
- **Audio Input for Dynamic Lighting Effects**
- **Spread-Spectrum Boost Converter**
- **100nA Shutdown Current**
- **Space-Saving, 4mm x 4mm, 24-Pin TQFN Package**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14521EETG+	-40°C to +85°C	24 TQFN-EP*

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Typical Operating Circuit



Quad, High-Voltage EL Lamp Driver with I²C Interface

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)
V_{DD} .....-0.3V to +6.0V
CS, EL1, EL2, EL3, EL4, COM.....-0.3V to +160V
LX .....-0.3V to +33V
RB, A0, A1, AUX.....-0.3V to +6.0V
SCL, SDA.....-0.3V to (V_{DD} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
24-Pin TQFN-EP (derate 27.8mW/°C above +70°C)..2222mW
Package Junction-to-Ambient Thermal Resistance (θ_{JA})
(Note 1) .....36°C/W
Package Junction-to-Case Thermal Resistance (θ_{JC})
(Note 1) .....3°C/W
Operating Temperature Range .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature.....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.5V, total C_{LAMP} = 10nF, C_{CS} = 3.3nF, tapped inductor = 2.3µH/115µH, 1:7 ratio (I_{SAT} = 0.7A, R_S = 1Ω), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{DD} = 3.7V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage	V_{DD}			2.7		5.5	V
Battery Voltage	V_{BAT}	(Note 3)				13.2	V
Input Supply Current	I_{DD}	All channels on, 300V_{P-P}, f_{EL} = 200Hz, sine-wave output shape			350	900	µA
Shutdown Supply Current	I_{SHDN}	RB, A0, A1 = 0V or V_{DD}; SCL = SDA = GND or V_{DD}; not toggling	T_A = +25°C		25	100	nA
			T_A = -40°C to +85°C			300	
Shutdown Tapped-Inductor Supply Current	I_{LX_SHDN}					2100	nA
Undervoltage Lockout	V_{UV}	V_{DD} rising		1.6	2.0	2.5	V
UVLO Hysteresis	V_{UV_HYST}				70		mV
EL OUTPUTS (EL_, COM)							
Peak-to-Peak Output Voltage	V_{P-P}	$V_{EL\_}$ - V_{COM}; EL_ _[4:0] = 01000; V_{DD} = 3.7V		66	78	90	V
		$V_{EL\_}$ - V_{COM}; EL_ _[4:0] = 10000; V_{DD} = 3.7V		136	154	172	
		$V_{EL\_}$ - V_{COM}; EL_ _[4:0] = 11111; V_{DD} = 3.7V		268	300	320	
Max Average Output Voltage	V_{AVG}	$V_{EL\_}$ - V_{COM}			1		V
EL_ High-Side Switch On-Resistance	$R_{ONHS\_EL\_}$				1270		Ω
EL_ Low-Side Switch On-Resistance	$R_{ONLS\_EL\_}$				700		Ω
COM High-Side Switch On-Resistance	R_{ONHS_COM}				390		Ω
COM Low-Side Switch On-Resistance	R_{ONLS_COM}				175		Ω

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, total C_{LAMP} = 10nF, C_{CS} = 3.3nF, tapped inductor = 2.3µH/115µH, 1:7 ratio (I_{SAT} = 0.7A, R_S = 1Ω), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{DD} = 3.7V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
EL_ High-Side Switch Off-Leakage	$I_{LKGHS\_EL\_}$			-1		+1	µA
EL_ Low-Side Switch Off-Leakage	$I_{LKGLS\_EL\_}$			-1		+1	µA
COM High-Side Switch Off-Leakage	I_{LKGHS_COM}			-1		+1	µA
COM Low-Side Switch Off-Leakage	I_{LKGLS_COM}			-1		+1	µA
EL Lamp Switching Frequency	f_{EL_LR}	FEL[7:0] = 1000 0000; V_{DD} = 3.7V	T_A = +25°C	194	200	206	Hz
			T_A = -40°C to +85°F	186	200	212	
	f_{EL_HR}	FEL[7:0] = 1011 1111; V_{DD} = 3.7V	T_A = +25°C	388	400	412	
			T_A = -40°C to +85°F	376	400	424	
BOOST CONVERTER							
Peak Output Voltage	V_{CS}	EL_ _[4:0] = 01000; V_{DD} = 3.7V		33	39	45	V
		EL_ _[4:0] = 10000; V_{DD} = 3.7V		68	77	86	
		EL_ _[4:0] = 11111; V_{DD} = 3.7V		134	150	160	
Tapped-Inductor Center Switching Frequency	f_{SW}	FSW[4:0] = 10000			400		kHz
		FSW[4:0] = 11111			800		
		FSW[4:0] = 00000 (default)			800		
		FSW[4:0] = 01111			1600		
Tapped-Inductor Switching Frequency Spreading Factor	S_F	SS[1:0] = 01, 10, or 11			8		%
Tapped-Inductor Switching Frequency Modulation Frequency	f_M	SS[1:0] = 11			f_{SW}/128		kHz
Switch On-Resistance	R_{LX}	I_{SINK} = 25mA, V_{DD} = 3.7V				3	Ω
LX Current	I_{LX}	V_{LX} = 30V		-1		+10	µA
CS Input Current	I_{CS}	No load, V_{CS} = 150V				27	µA
CONTROL INPUT AUX							
Input Range	AUX_{RNG}			0		V_{DD}	V
Input Capacitance	AUX_{CAP}				10		pF
CONTROL INPUT RB							
Input Logic-Low Voltage	V_{IL_RB}					0.5	V
Input Logic-High Voltage	V_{IH_RB}			1.5			V
Input Hysteresis	I_{HYS_RB}				130		mV
Input Leakage Current	I_{LKG_RB}	V_{RB} = 5.5V or 0		-1		+1	µA
Input Capacitance	C_{IN}				10		pF
I²C INTERFACE LOGIC (SDA, SCL, A1, AND A0) (Figure 1)							
Input Logic-Low Voltage	V_{IL}					0.5	V
Input Logic-High Voltage	V_{IH}			1.5			V
Input Hysteresis	I_{HYS}				130		mV

Quad, High-Voltage EL Lamp Driver with I²C Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.5V, total C_{LAMP} = 10nF, C_{CS} = 3.3nF, tapped inductor = 2.3µH/115µH, 1:7 ratio (I_{SAT} = 0.7A, R_S = 1Ω), T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C and V_{DD} = 3.7V.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{LKG}		-1		+1	µA
Output Low Voltage	V_{OL}	I_{SINK} = 3mA			0.4	V
Input/Output Capacitance	$C_{I/O}$			10		pF
Serial-Clock Frequency	f_{SCL}				400	kHz
Clock Low Period	t_{LOW}		1.3			µs
Clock High Period	t_{HIGH}		0.6			µs
Bus Free Time	t_{BUF}		1.3			µs
START Setup Time	$t_{SU,STA}$		0.6			µs
START Hold Time	$t_{HD,STA}$		0.6			µs
STOP Setup Time	$t_{SU,STO}$		0.6			µs
Data In Setup Time	$t_{SU,DAT}$		100			ns
Data In Hold Time	$t_{HD,DAT}$		0		900	ns
Receive SCL/SDA Minimum Rise Time	t_R			$20 + 0.1C_B$		ns
Receive SCL/SDA Maximum Rise Time	t_R			300		ns
Receive SCL/SDA Minimum Fall Time	t_F			$20 + 0.1C_B$		ns
Receive SCL/SDA Maximum Fall Time	t_F			300		ns
Transmit SDA Fall Time	t_F	C_B = 400pF	$20 + 0.1C_B$		300	ns
SCL/SDA Noise Suppression Time	t_I			50		ns
ESD PROTECTION						
EL_, COM		Human Body Model		±15		kV
		IEC 61000-4-2 Contact Discharge		±6		
		IEC 61000-4-2 Air Gap Discharge		±8		
THERMAL PROTECTION						
Thermal Shutdown	T_{SHDN}			160		°C
Thermal Shutdown Hysteresis	T_{HYST}			12		°C

Note 2: All parameters are 100% production tested at T_A = +25°C and T_A = +85°C, unless otherwise noted. Parameters at -40°C are guaranteed by design.

Note 3: See the *f_{SW} Selection* section when V_{BAT} is above 5.5V.

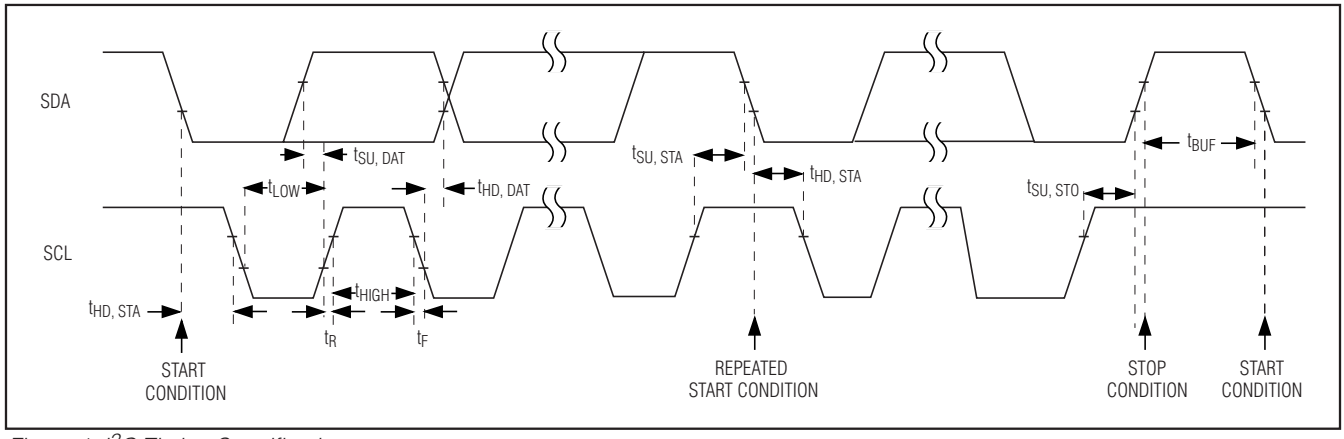
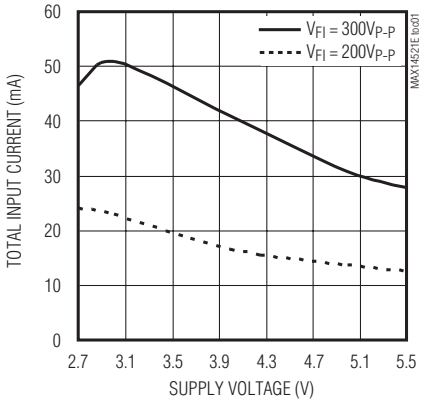


Figure 1. I²C Timing Specifications

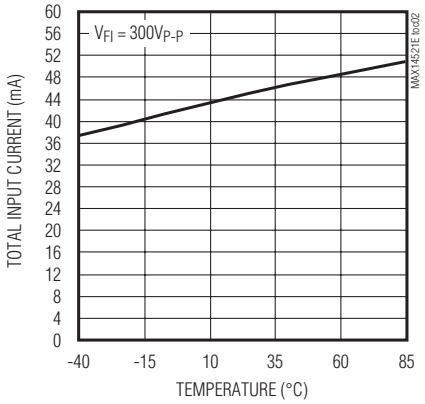
Typical Operating Characteristics

(V_{DD} = 3.7V, total C_{LAMP} = 10nF, C_{CS} = 3.3nF, L_X = 2.3µH/115µH, 1:7 ratio, (I_{SAT} = 0.7A, R_S = 1Ω), T_A = +25°C, sine-wave output, f_{SW} = 800kHz, f_{EL} = 200Hz, unless otherwise noted.)

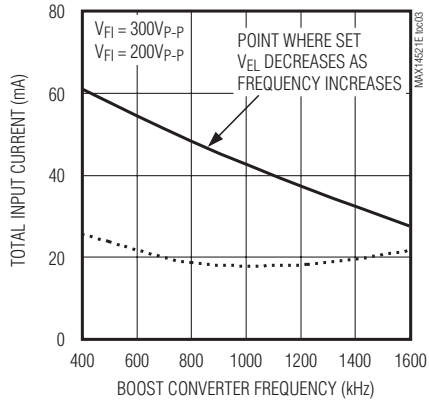
TOTAL INPUT CURRENT vs. SUPPLY VOLTAGE



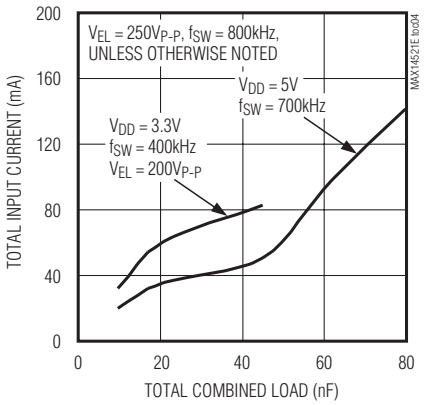
TOTAL INPUT CURRENT vs. TEMPERATURE



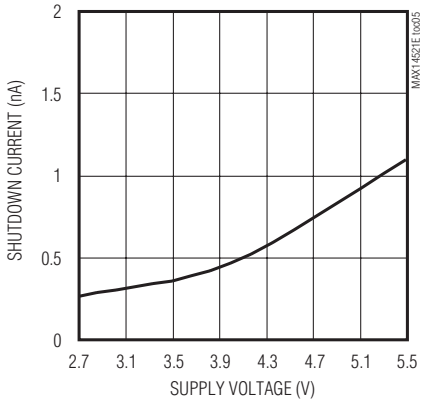
TOTAL INPUT CURRENT vs. BOOST CONVERTER FREQUENCY



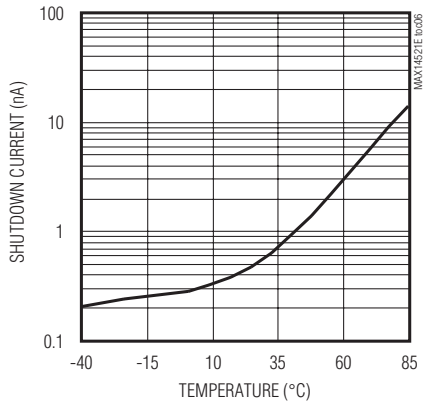
TOTAL INPUT CURRENT vs. LOAD



SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



SHUTDOWN CURRENT vs. TEMPERATURE

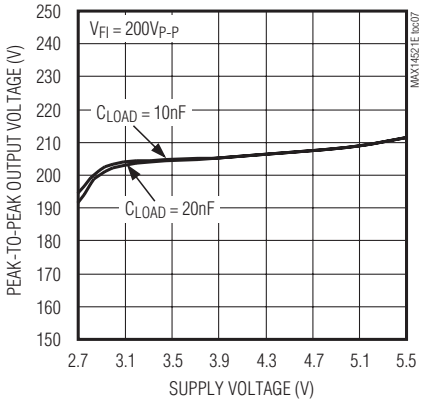


Quad, High-Voltage EL Lamp Driver with I²C Interface

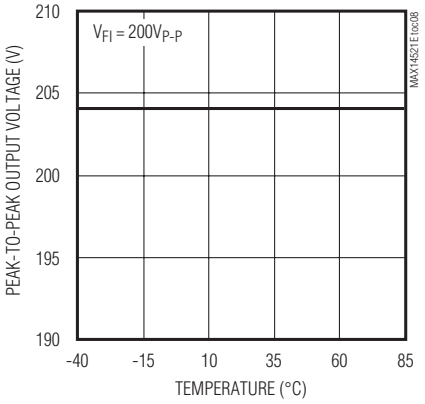
Typical Operating Characteristics (continued)

(V_{DD} = 3.7V, total C_{LAMP} = 10nF, C_{CS} = 3.3nF, L_X = 2.3µH/115µH, 1:7 ratio, (I_{SAT} = 0.7A, R_S = 1Ω), T_A = +25°C, sine-wave output, f_{SW} = 800kHz, f_{EL} = 200Hz, unless otherwise noted.)

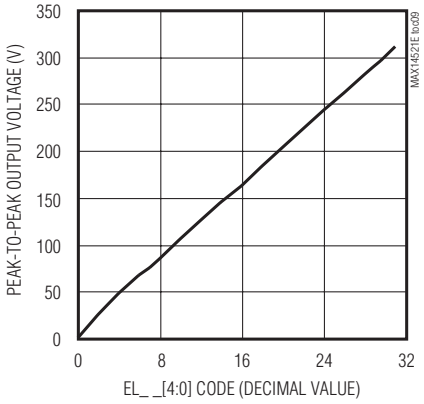
PEAK-TO-PEAK OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



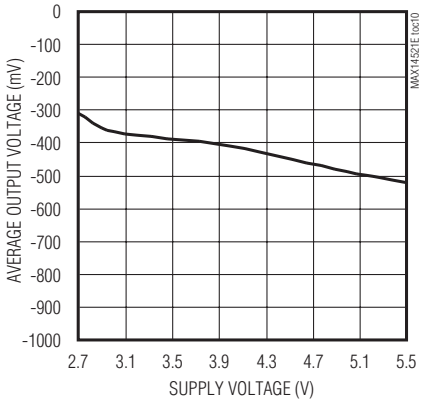
PEAK-TO-PEAK OUTPUT VOLTAGE vs. TEMPERATURE



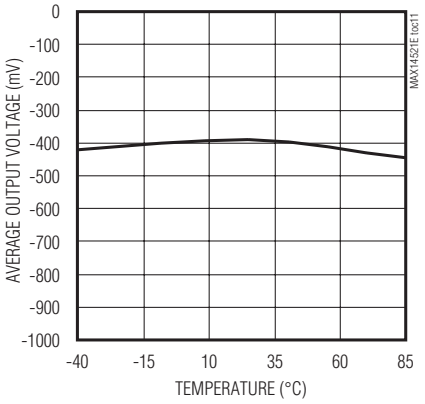
PEAK-TO-PEAK OUTPUT VOLTAGE vs. CODE



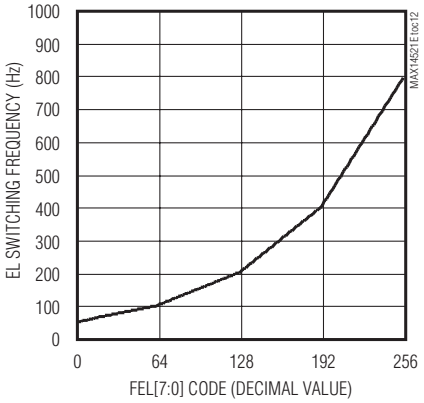
AVERAGE OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



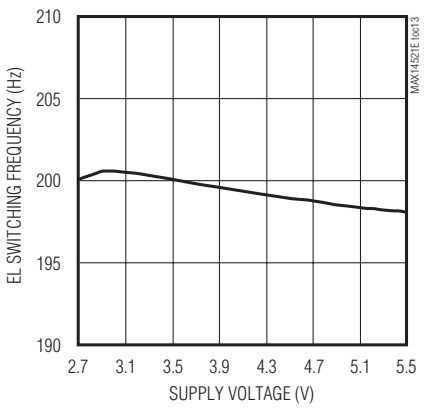
AVERAGE OUTPUT VOLTAGE vs. TEMPERATURE



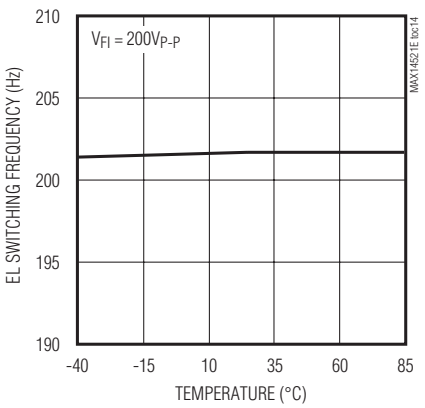
EL SWITCHING FREQUENCY vs. FEL[7:0]



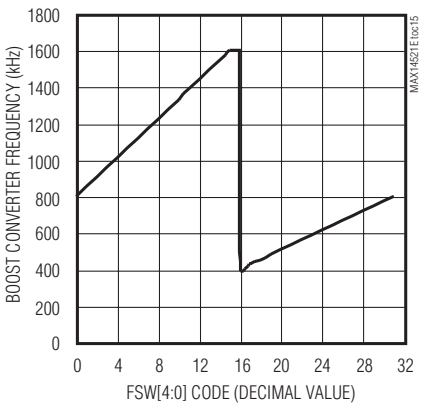
EL SWITCHING FREQUENCY vs. SUPPLY VOLTAGE



EL SWITCHING FREQUENCY vs. TEMPERATURE



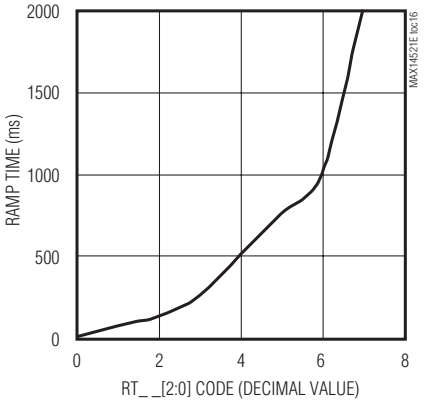
BOOST CONVERTER FREQUENCY vs. FSW[4:0]



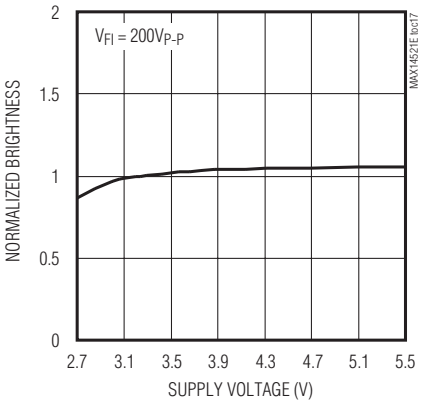
Typical Operating Characteristics (continued)

(V_{DD} = 3.7V, total C_{LAMP} = 10nF, C_{CS} = 3.3nF, L_X = 2.3µH/115µH, 1:7 ratio, (I_{SAT} = 0.7A, R_S = 1Ω), T_A = +25°C, sine-wave output, f_{SW} = 800kHz, f_{EL} = 200Hz, unless otherwise noted.)

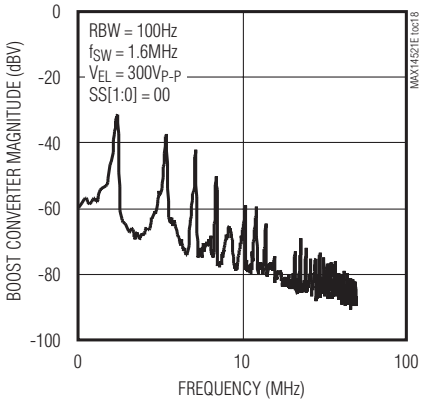
RAMP TIME vs. CODE



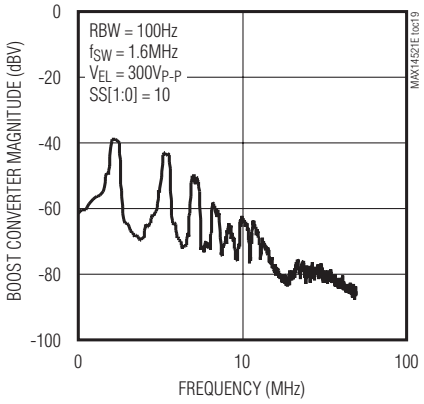
NORMALIZED BRIGHTNESS vs. SUPPLY VOLTAGE



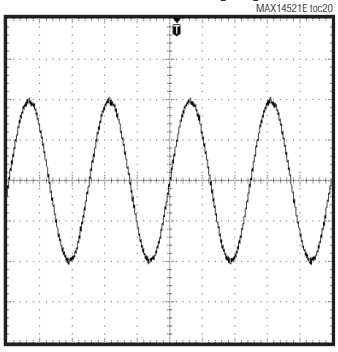
BOOST CONVERTER MAGNITUDE vs. FREQUENCY (SPREAD SPECTRUM DISABLED)



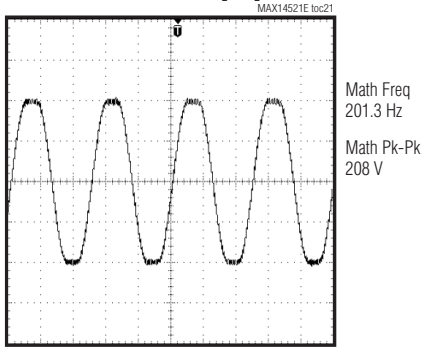
BOOST CONVERTER MAGNITUDE vs. FREQUENCY (SPREAD SPECTRUM ENABLED)



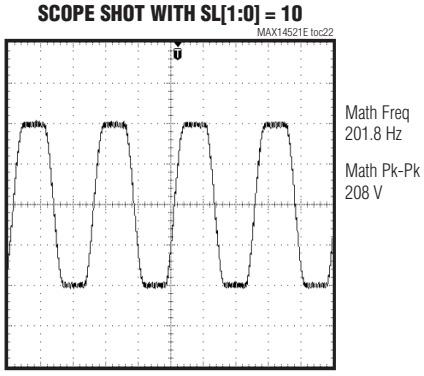
SCOPE SHOT WITH SL[1:0] = 00



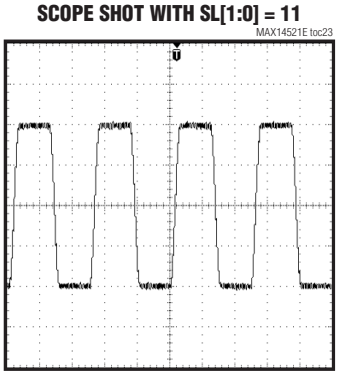
SCOPE SHOT WITH SL[1:0] = 01



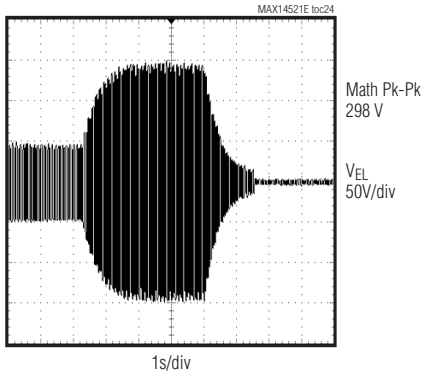
SCOPE SHOT WITH SL[1:0] = 10



SCOPE SHOT WITH SL[1:0] = 11



RAMPING TIME



Quad, High-Voltage EL Lamp Driver with I²C Interface

Pin Description

PIN	NAME	FUNCTION
1	EL1	High-Voltage EL Panel Output 1. Connect EL1 to segment 1 of the EL lamp.
2, 4, 16, 18, 20, 22, 24	N.C.	No Connection. Not internally connected.
3	CS	Feedback Connection. Connect CS to the output of the boost converter (cathode of the rectifying diode).
5	LX	Internal Switching DMOS Drain Connection. Connect LX to the middle terminal of the tapped inductor.
6	PGND	Power Ground. Connect to GND.
7	A0	Address Input 0. Address inputs allow up to four connections on one common bus. Connect A0 to GND or V_{DD}.
8	A1	Address Input 1. Address inputs allow up to four connections on one common bus. Connect A1 to GND or V_{DD}.
9	V_{DD}	Input Supply Voltage
10	SDA	Open-Drain, Serial Data Input/Output. SDA requires an external pullup resistor.
11	SCL	Serial-Clock Input. SCL requires an external pullup resistor.
12	RB	Reset Input. Drive RB low to clear all registers to zero and put the device into a low-power shutdown mode. The device does not respond to I²C communications when RB is held low.
13	AUX	Audio Effects Input. Modulates amplitude/frequency of the EL output with the AUX input voltage amplitude.
14	I.C.	Internally Connected. Connect I.C. to GND.
15	GND	Ground
17	EL4	High-Voltage EL Panel Output 4. Connect EL4 to segment 4 of the EL lamp.
19	EL3	High-Voltage EL Panel Output 3. Connect EL3 to segment 3 of the EL lamp.
21	COM	High-Voltage COM Output. Connect COM to common terminal of the EL lamp.
23	EL2	High-Voltage EL Panel Output 2. Connect EL2 to segment 2 of the EL lamp.
—	EP	Exposed Pad. Connect EP to GND.

Detailed Description

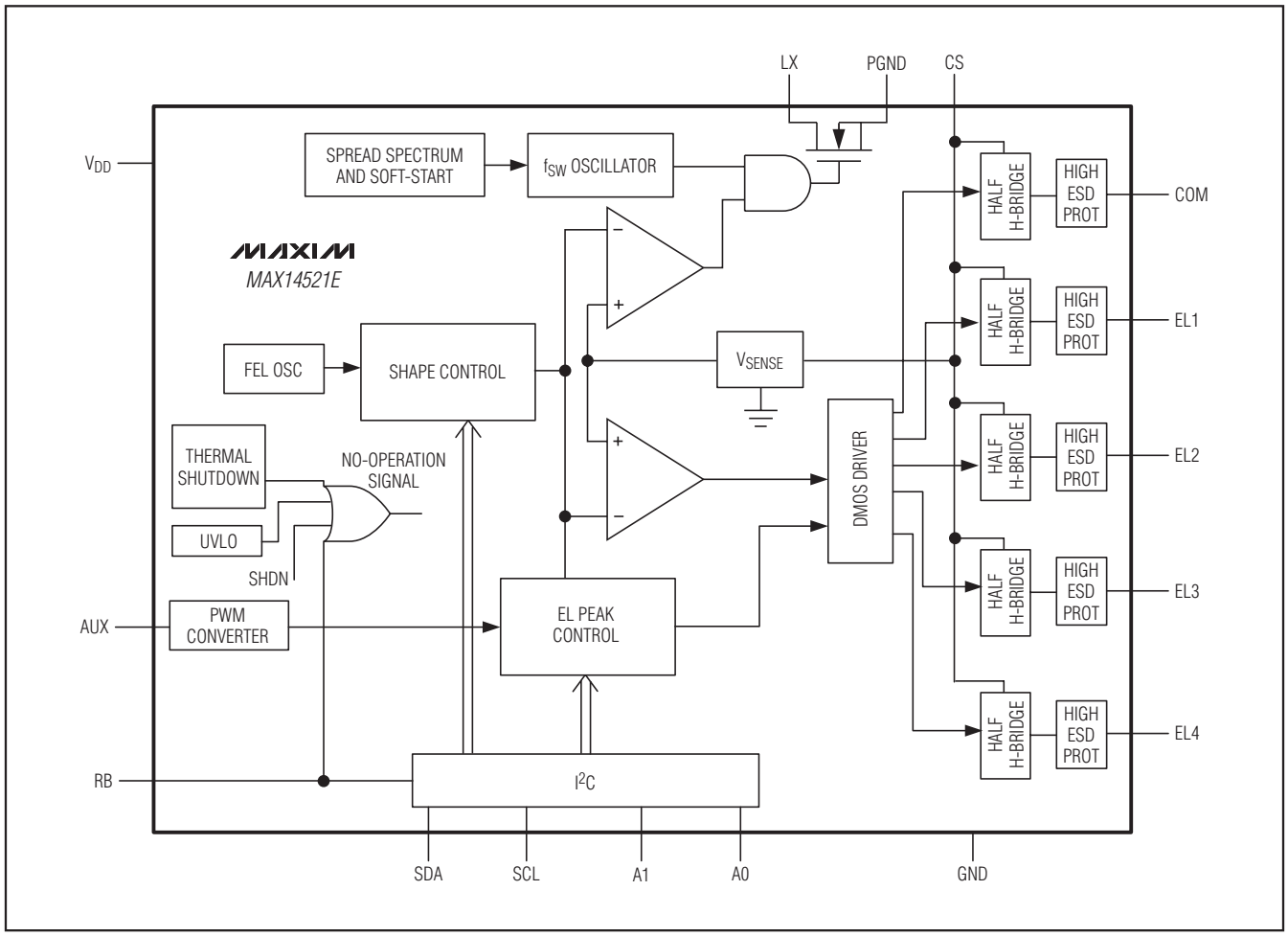
The MAX14521E is a quad-output high-voltage DC-AC converter that drives four EL lamps. The device features a 2.7V to 5.5V input range that allows the device to accept a variety of sources such as single-cell Li+ batteries. The lamp outputs of the device generate up to $300V_{P-P}$ for maximum lamp brightness.

The MAX14521E utilizes a high-frequency spread-spectrum boost converter that reduces the amount of EMI/EFI generated by the circuit. The boost-converter switching frequency is set with an 8-bit register through the I²C interface. The MAX14521E uses a high-voltage full-bridge output stage to convert the high voltage generated by the boost converter to an AC waveform suitable for driving an EL lamp. An internal register controlled through the I²C interface sets the shape of the EL output waveshape.

The EL output switching frequency for all outputs is set with an 8-bit register through the I²C interface. The MAX14521E provides a serial digital interface that allows the user to set the peak voltage of each output independently with 5 bits of resolution. The MAX14521E also provides an adjustable automatic ramping feature that slowly increases or decreases the peak output voltage when the set value is changed. The slew rate of the ramp is set with 3 bits of resolution through the I²C interface and it is independent for each channel. The MAX14521E features an audio auxiliary input AUX that modulates the EL output voltage and frequency for dynamic lighting effects.

The high-voltage outputs are ESD protected up to ±15kV Human Body Model, ±8kV Air Gap Discharge, and ±6kV Contact Discharge, as specified in IEC 61000-4-2.

Functional Diagram



EL Output Voltage

The shape, slope, frequency, ramp-on/-off times, and peak-to-peak voltage of the MAX14521E lamp outputs are programmed using internal registers.

The MAX14521E is capable of producing output waveforms with varying shapes and slew rates. The user sets the shape and slew rate of the output using bits in the EL shape registers.

The MAX14521E EL lamp output frequency uses an internal EL oscillator to set the desired frequency. The output frequency is adjusted by the FEL[7:0] bits of the EL output frequency register. The EL frequency increases and decreases linearly with FEL[7:0].

The peak-to-peak voltage of the EL lamp output is varied from 0 to 300V_{P-P} by programming the EL_ _[4:0] bits of the EL ramping time and EL peak voltage registers. The peak-to-peak voltage increases and decreases linearly with EL_ _[4:0].

The MAX14521E also features a slow fade-on and slow fade-off time feature programmed by the RT_ _ [2:0] bits of the EL ramping time and EL peak voltage registers. This slow fade-on/-off feature causes the peak-to-peak voltage of the EL outputs to slowly rise from the previously set value to the maximum set value. This feature also causes the peak-to-peak voltage of the EL outputs to fall from the maximum set value to zero when the device is placed into shutdown. The slow rise and fall of the peak-to-peak EL output voltage creates a soft fade-on and fade-off of the EL lamp.

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Boost Converter

The MAX14521E boost converter consists of an external-tapped inductor from V_{DD} to the LX input, an internal DMOS switch, an external diode from the secondary of the tapped inductor to the CS output, an external capacitor from the CS output to GND, and an EL lamp connected to the EL lamp outputs. When the DMOS switch is turned on, LX is connected to GND, and the inductor is charged. When the DMOS switch is turned off, the energy stored in the inductor is transferred to the capacitor C_{CS} and the EL lamp.

Note: The MAX14521E exhibits high-voltage spikes on the LX node. The addition of a snubber circuit to the LX node protects the device by suppressing the high-voltage spikes. The values of R_{SN} and C_{SN} should be optimized for the specific tapped inductor used. Typical values are R_{SN} = 20Ω and C_{SN} = 330pF.

The MAX14521E boost-converter frequency uses an internal oscillator to set the frequency of the boost converter. The oscillator frequency is adjusted by the FSW[4:0] bits of the boost-converter frequency register. The boost converter increases and decreases linearly with FSW[3:0].

To further reduce the amount of EMI/EFI generated by the circuit, the boost-converter frequency can be modulated (see the SS[1:0] bits of the boost-converter frequency register). Enabling modulation spreads the switching energy of the oscillator in the frequency domain, thus decreasing EMI.

Independent Dimming Control

The brightness of an EL lamp is proportional to the peak-to-peak voltage applied across the lamp. The MAX14521E provides four registers to control the EL peak-to-peak voltage of each EL output using the EL_ _[4:0] bits of the EL ramping time and EL peak voltage registers.

EL Output Waveshape

The MAX14521E can produce sine-wave to square-wave waveshapes on the EL output by varying the slope of the EL output. This is achieved by using bits SL[1:0] of the EL shape register. If the EL shape configuration is set to sine and if all EL outputs have the same amplitude settings, then each EL output has a sinusoidal waveshape. If the EL outputs have different amplitude settings, then the EL output with the highest setting has a sine waveshape while the remaining EL outputs have a clamped sine waveshape.

Auxiliary Audio Input (AUX)

The MAX14521E uses an auxiliary input AUX that accepts an audio signal to produce visual effects on the EL outputs. The frequency and amplitude modulation (FR_AM) bit is set to modulate the EL output voltage or frequency. The AUX audio signal modulates the EL output voltage when FR_AM is set to 0 and modulates the EL output frequency when FR_AM is set to 1.

When the NO_SAMPLE bit is enabled, the voltage of the EL outputs is proportional to the voltage at AUX. For example, when FR_AM = 0, NO_SAMPLE = 1, and any of the AU1, AU2, AU3, AU4 bits are set to 1, the peak value of those particular channels follow AUX directly.

If AUX is a DC value, the EL output voltage is V_{EL} = 250 x AUX (V_{P-P}) with a maximum of 300V_{P-P}.

AUX can also accept a PWM signal with a frequency ranging from 100kHz to 10MHz, where the EL output voltage is V_{EL} = 300 x DutyCycle% (V_{P-P}). The NO_SAMPLE bit has no effect when FR_AM = 1.

When FR_AM = 1, frequency modulation is enabled and the AUXDIV1 and AUXDIV0 bits are used to divide the audio frequency and apply this to the EL outputs. AU1, AU2, AU3, and AU4 must be set to 1 to enable this feature.

Shutdown

The MAX14521E features two methods to place the device in shutdown: 1) a reset input, RB, to clear all registers to zero and put the device into low-power shutdown mode, and 2) the EN bit of the system register. Using method 1, the device does not respond to I²C communications when RB is held low. Using method 2, the EL outputs are shut down; however, the register contents remain unchanged.

Undervoltage Lockout (UVLO)

The MAX14521E has a UVLO threshold of +2.0V (typ). When V_{DD} falls below +2.0V (typ), the device enters a nonoperative mode. The contents of the I²C registers are not guaranteed below UVLO.

Thermal Protection

The MAX14521E enters a nonoperative mode if the internal die temperature of the device reaches or exceeds +160°C (typ). The MAX14521E is latched, and only placing RB to 0 resets the thermal protection bit as well as all registers.

I²C Registers and Bit Descriptions

Ten internal registers program the MAX14521E. Table 1 lists all the registers, their addresses, and power-on reset states. All registers are read/write. Register 0x0A is reserved as a command to update all EL peak voltage output registers. Register 0x0B is reserved and should not be written to.

Table 1. Register Map

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS	POWER-ON RESET STATE
SYSTEM										
Device ID	DEVID3	DEVID2	DEVID1	DEVID0	REV3	REV2	REV1	REV0	0x00	0xB2
Power Mode	OVR TEMP*	X	X	X	X	X	X	EN	0x01	0x00
EL FREQUENCY										
EL Output Frequency	FEL7	FEL6	FEL5	FEL4	FEL3	FEL2	FEL1	FEL0	0x02	0x00
EL SHAPE										
Slope/Shape	X	ENDAMP	X	X	SHAPE1	SHAPE0	SL1	SL0	0x03	0x00
BOOST-CONVERTER FREQUENCY										
Boost-Converter Frequency	SS1	SS0	X	FSW4	FSW3	FSW2	FSW1	FSW0	0x04	0x00
AUDIO										
Audio Effects	FR_AM	NO_ SAMPLE	AUXDIV1	AUXDIV0	AU4	AU3	AU2	AU1	0x05	0x00
EL RAMPING TIME AND EL PEAK VOLTAGE										
EL1 Ramping Time and EL Peak Voltage**	RT1_2	RT1_1	RT1_0	EL1_4	EL1_3	EL1_2	EL1_1	EL1_0	0x06	0x00
EL2 Ramping Time and EL Peak Voltage**	RT2_2	RT2_1	RT2_0	EL2_4	EL2_3	EL2_2	EL2_1	EL2_0	0x07	0x00
EL3 Ramping Time and EL Peak Voltage**	RT3_2	RT3_1	RT3_0	EL3_4	EL3_3	EL3_2	EL3_1	EL3_0	0x08	0x00
EL4 Ramping Time and EL Peak Voltage**	RT4_2	RT4_1	RT4_0	EL4_4	EL4_3	EL4_2	EL4_1	EL4_0	0x09	0x00

X = Don't Care

**Read back only.*

***Send command 0Ah (update all EL ramping time and EL peak voltage registers) to have the programmed voltage effectively applied to the EL lamp.*

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Slave Address

The MAX14521E device address is set through external inputs. The slave address consists of five fixed bits (B7–B3, set to 11110) followed by two input programmable bits (A1 and A0).

For example: If A1 and A0 are hardwired to ground, then the complete address is 1111000. The full address is defined as the seven most significant bits followed by the read/write bit. Set the read/write bit to 1 to configure the MAX14521E to read mode. Set the read/write bit to 0 to configure the MAX14521E to write mode. The address is the first byte of information sent to the MAX14521E after the START condition.

System Registers (0x00, 0x01)

Device ID (DEVID3/DEVID2/DEVID1/DEVID0)

DEVID[3:0] is preprogrammed to 1011 to identify the MAX14521E; see Table 2.

Revision (REV3/REV2/REV1/REV0)

REV[3:0] is preprogrammed to the current revision of the MAX14521E and is REV[3:0] = 0010.

System Overtemperature (OVRTEMP)

1 = Thermal shutdown temperature exceeded.

0 = Analog circuitry operating properly.

OVRTEMP = 1 turns the EL outputs off. To set OVRTEMP to 0 and restart in default condition (all register reset), the user must place RB = 0.

System Enable (EN)

1 = EL outputs enabled.

0 = EL outputs disabled.

EN = 1 places the MAX14521E in a normal operating mode. Register contents are restored to values prior to shutdown. EN = 0 disables the EL outputs and places the device in a low-power shutdown state.

EL Frequency Register (0x02)

EL Frequency (FEL[7:0])

FEL[7:6] sets the EL frequency range of all EL outputs and FEL[5:0] sets the EL frequency within the frequency range; see Table 4. FEL[5:0] = 000000 sets the frequency to the minimum value of the frequency range. FEL[5:0] = 111111 sets the frequency to the maximum value of the frequency range. EL frequency increases linearly with FEL[5:0]; see Table 3.

Table 2. Device Identification, Status, and Enable

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x00	DEVID3	DEVID2	DEVID1	DEVID0	REV3	REV2	REV1	REV0
0x01	OVRTEMP	X	X	X	X	X	X	EN

X = Don't Care

Table 3. EL Output Frequency

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x02	FEL7	FEL6	FEL5	FEL4	FEL3	FEL2	FEL1	FEL0

Table 4. EL Frequency Range

FEL[7:6]	EL FREQUENCY RANGE (Hz)
00	50–100
01	100–200
10	200–400
11	400–800

EL Shape Register (0x03)

Damping Enable (ENDAMP)

1 = Active damping on LX node enabled.

0 = Active damping on LX node disabled.

ENDAMP = 1 actively damps the oscillation on the LX pin and could reduce EMI.

EL Shape (SHAPE1/SHAPE0)

SHAPE[1:0] sets the desired EL output waveform; see Tables 5 and 6.

EL Slew Rate (SL1/SL0)

SL[1:0] sets the slope of the EL output; see Table 7.

Boost-Converter Frequency Register (0x04)

Spread Spectrum (SS1/SS0)

SS[1:0] sets the spread-spectrum modulation frequency to a fraction of the boost-converter frequency; see Tables 8 and 9.

Boost-Converter Switching Frequency (FSW[4:0])

FSW4 sets the switching frequency range of the boost converter and FSW[3:0] sets the switching frequency within the frequency range; see Table 10. The frequency range for FSW4 = 0 is 800kHz–1600kHz. The frequency range for FSW4 = 1 is 400kHz–800kHz. FSW[3:0] = 0000 sets the frequency to the minimum value of the frequency range. FSW[3:0] = 1111 sets the frequency to the maximum value of the frequency range. Boost-converter switching frequency increases linearly with FSW[3:0].

Table 5. EL Shape Configuration

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x03	X	ENDAMP	X	X	SHAPE1	SHAPE0	SL1	SL0

X = Don't Care

Table 6. EL Output Shape Configuration

SHAPE[1:0]	EL OUTPUT SHAPE
0X	Sine
10	Do Not Use
11	Do Not Use

X = Don't Care

Table 7. EL Slope Configuration

SL[1:0]	EL OUTPUT SLOPE
00	Sine
01	Fast Slope
10	Faster Slope
11	Fastest Slope (Square Wave)

Table 8. Boost-Converter Configurations

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x04	SS1	SS0	X	FSW4	FSW3	FSW2	FSW1	FSW0

X = Don't Care

Table 9. Spread-Spectrum Configuration

SS[1:0]	SPREAD SPECTRUM
00	Disabled
01	1/8
10	1/32
11	1/128

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Audio Input Register (0x05)

Frequency and Amplitude Modulation (FR_AM)

0 = AUX input signal modulates EL output voltage.

1 = AUX input frequency modulates EL output frequency.

AUX Envelope on EL Output (NO_SAMPLE)

1 = The EL output envelope follows that of the AUX envelope.

0 = AUX is sampled every f_{EL} cycle and the corresponding EL output cycle has zero DC average.

Set FR_AM = 0 when NO_SAMPLE = 1 and enable the corresponding EL outputs by bits AU[4:1]. If FR_AM = 1, the NO_SAMPLE bit has no effect. If AUX is a DC value, the EL output peak-to-peak voltage is EL_ (V_{P-P}) = 250 x AUX (V) with a maximum of 300V_{P-P}. If AUX is a PWM signal with a frequency from 100kHz to 10MHz, the EL output voltage is V_{EL} = 300 x DutyCycle% (V_{P-P}).

Table 10. Boost-Converter Frequency Range

FSW3	FSW2	FSW1	FSW0	BOOST-CONVERTER SWITCHING FREQUENCY (kHz)	
				FSW4 = 0	FSW4 = 1
0	0	0	0	800	400
0	0	0	1	853	427
0	0	1	0	907	453
0	0	1	1	960	480
0	1	0	0	1013	507
0	1	0	1	1067	533
0	1	1	0	1120	560
0	1	1	1	1173	587
1	0	0	0	1227	613
1	0	0	1	1280	640
1	0	1	0	1333	667
1	0	1	1	1387	693
1	1	0	0	1440	720
1	1	0	1	1493	747
1	1	1	0	1547	773
1	1	1	1	1600	800

Table 11. Audio Input Configurations

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x05	FR_AM	NO_ SAMPLE	AUXDIV1	AUXDIV0	AU4	AU3	AU2	AU1

Frequency Divider (AUXDIV1/AUXDIV0)

AUXDIV[1:0] sets the divisor to divide down the AUX input frequency; see Table 12.

Audio Enable (AU4/AU3/AU2/AU1)

1 = Enable audio effect to EL output.

0 = Disable audio effect to EL output.

When FR_AM = 0 the EL outputs can be enabled and disabled independently according to AU[4:1]. When FR_AM = 1 then all AU[4:1] bits must be set to 1 (i.e. AU[4:1] = 1111) to enable the audio effect on the EL outputs.

EL Peak Ramping Time and EL Peak Voltage Register (0x06, 0x07, 0x08, 0x09)

EL Ramping Time (RT4_ _/RT3_ _/RT2_ _/RT1_ _)

RT_ _[2:0] sets the ramp time of each EL output; see Table 14.

EL Peak-to-Peak Voltage (EL1_ _/EL2_ _/EL3_ _/EL4_ _)

EL _ _[4:0] controls the peak-to-peak voltage of each EL output. When EL _ _[4:0] = 00000, the EL output follows COM. When EL_ _[4:0] = 11111, the EL output has a 150V peak with respect to COM. The EL output voltage rises linearly with EL_ _[4:0].

I²C Interface

The MAX14521E features an I²C-compatible as a slave device, 2-wire serial interface consisting of a serial data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication to the device at clock rates up to 400kHz. Figure 1 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. A master device writes data to the MAX14521E by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX14521E is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX14521E transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX14521E from high-voltage spikes on the bus lines, and minimize crosstalk and undershoot of the bus signals.

Table 12. AUX Frequency Divider Configuration

AUXDIV[1:0]	AUX FREQUENCY DIVIDER
00	16
01	8
10	4
11	2

Table 13. EL Output Configuration

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0
0x06	RT1_2	RT1_1	RT1_0	EL1_4	EL1_3	EL1_2	EL1_1	EL1_0
0x07	RT2_2	RT2_1	RT2_0	EL2_4	EL2_3	EL2_2	EL2_1	EL2_0
0x08	RT3_2	RT3_1	RT3_0	EL3_4	EL3_3	EL3_2	EL3_1	EL3_0
0x09	RT4_2	RT4_1	RT4_0	EL4_4	EL4_3	EL4_2	EL4_1	EL4_0

Table 14. Ramping Time Configuration

RT_ _[2:0]	RAMPING TIME (ms)
000	< 0.1
001	62.5
010	125
011	250
100	500
101	750
110	1000
111	2000

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Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *START and STOP Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 2). A START condition from the master signals the beginning of a transmission to the MAX14521E. The master terminates transmission and frees the bus by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

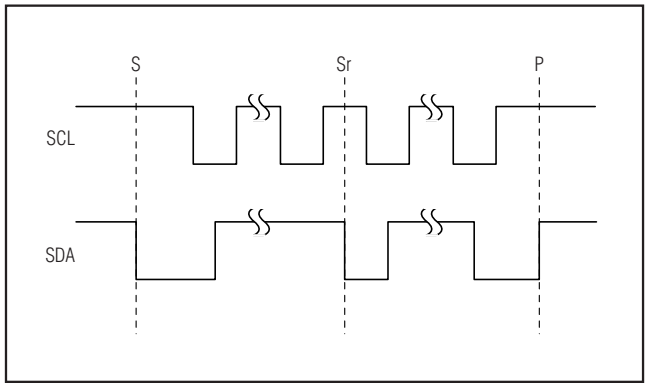

Figure 2. START, STOP, and REPEATED START Conditions

Early STOP Conditions

The MAX14521E recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The MAX14521E has selectable device addresses through external inputs. The slave address consists of five fixed bits (B7–B3, set to 11110) followed by two pin programmable bits (A1 and A0).

For example: If A1 and A0 are hardwired to ground, the complete address is 1111000. The full address is defined as the seven most significant bits followed by the read/write bit. Set the read/write bit to 1 to configure the MAX14521E to read mode. Set the read/write bit to 0 to configure the MAX14521E to write mode. The address is the first byte of information sent to the MAX14521E after the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX14521E uses to handshake receipt each byte of data when in write mode (see Figure 3). The MAX14521E pull down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault had occurred. In the event of an unsuccessful data transfer, the bus master may retry communication.

The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX14521E are in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX14521E followed by a STOP condition.

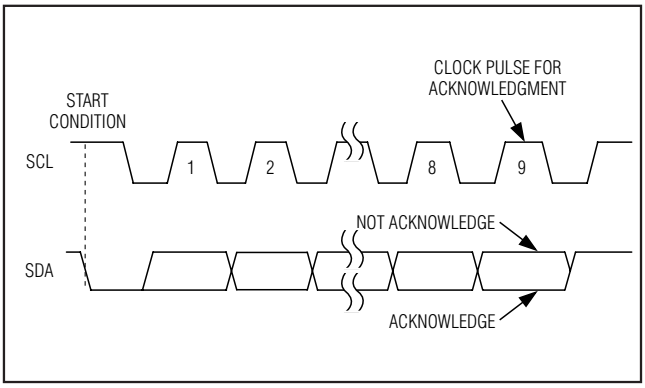

Figure 3. Acknowledge

Write Data Format

A write to the MAX14521E includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, one byte of data to configure the internal register address pointer, one or more bytes of data, and a STOP condition. Figure 4 illustrates the proper frame format for writing one byte of data to the MAX14521E. Figure 5 illustrates the frame format for writing n-bytes of data to the MAX14521E.

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX14521E. The MAX14521E acknowledge receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the MAX14521E internal register address pointer. The pointer tells the MAX14521E where to write the next byte of data. An acknowledge pulse is sent by the MAX14521E upon receipt of the address pointer data.

The third byte sent to the MAX14521E contains the data that will be written to the chosen register. An acknowledge pulse from the MAX14521E signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. Attempting to write to register addresses higher than 0x0B results in repeated writes of 0x0B. Figure 5 illustrates how to write to multiple registers with one frame. The master signals the end of transmission by issuing a STOP condition.

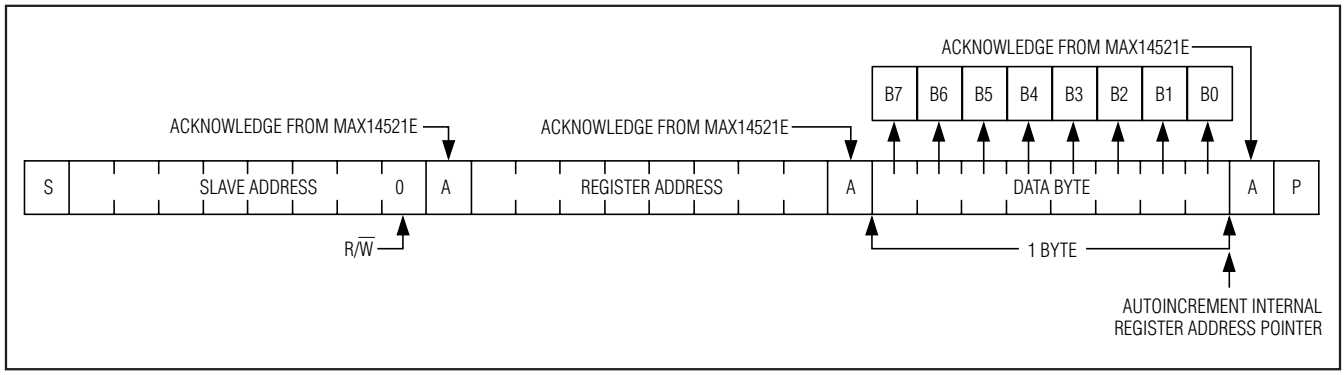

Figure 4. Writing One Byte of Data to the MAX14521E

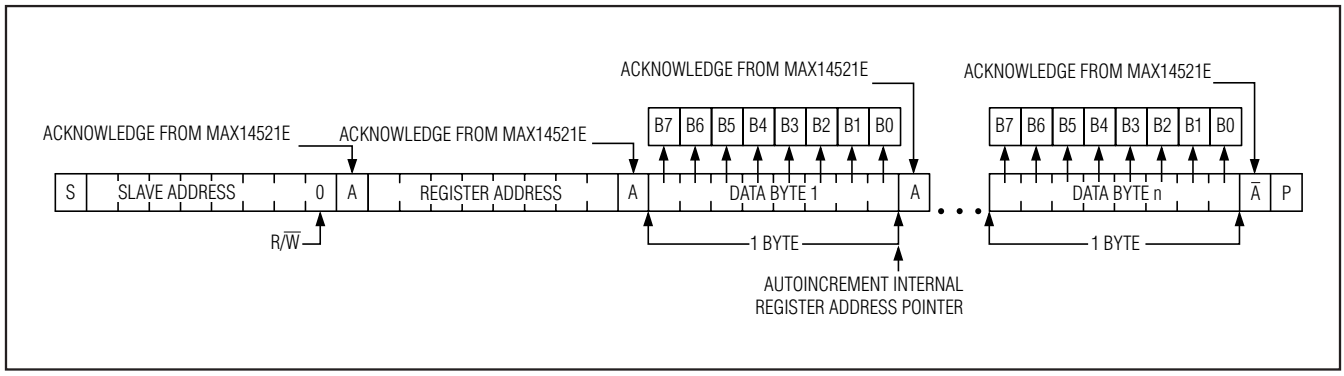

Figure 5. Writing n-Bytes of Data to the MAX14521E

Quad, High-Voltage EL Lamp Driver with I²C Interface

Read Data Format

Send the slave address with the R/$\overline{W}$ set to 1 to initiate a read operation. The MAX14521E acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00. The first byte transmitted from the MAX14521E will be the contents of register 0x00. Transmitted data is valid on the rising edge of the master-generated serial clock (SCL). The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read will be from register 0x00 and subsequent reads will autoincrement the address pointer until the next STOP condition. The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX14521E's slave address with the R/$\overline{W}$ bit set to 0 followed by the register address. A REPEATED START condition is then sent, followed by the slave address with the R/$\overline{W}$ set to 1. The MAX14521E transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte. Attempting to read from register addresses higher than 0x0B results in repeated reads of 0x0B. The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 6 illustrates the frame format for reading one byte from the MAX14521E. Figure 7 illustrates the frame format for reading multiple bytes from the MAX14521E.

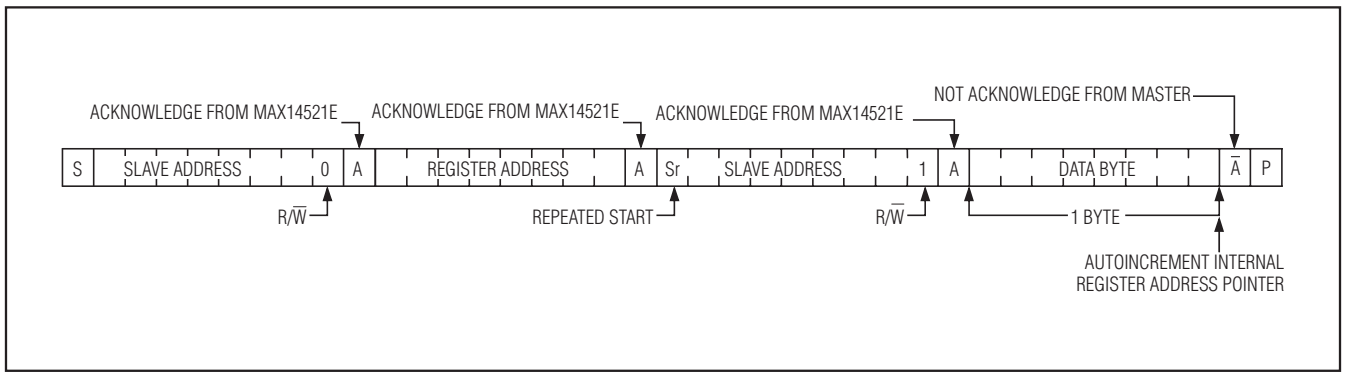

Figure 6. Reading One Indexed Byte of Data from the MAX14521E

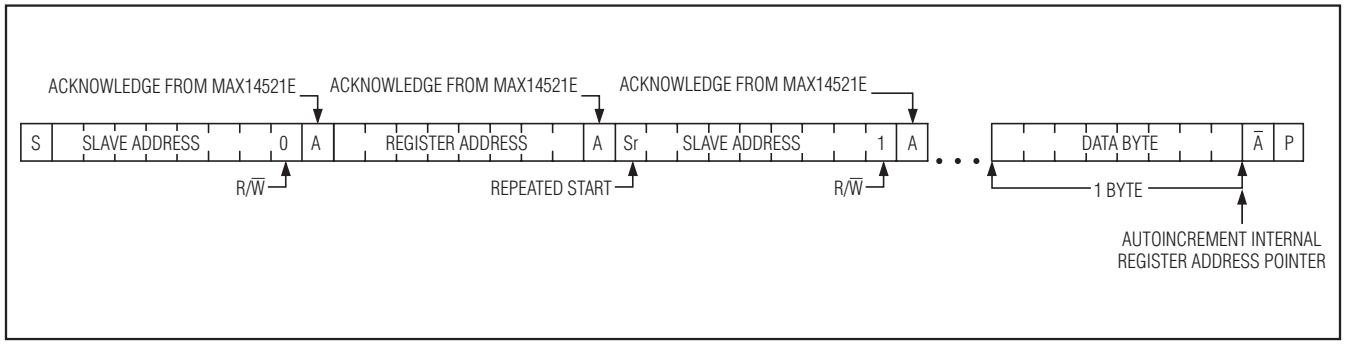

Figure 7. Reading n-Bytes of Indexed Data from the MAX14521E

ESD Test Conditions

ESD performance depends on a number of conditions. The MAX14521E are specified for ±15kV (HBM) typical ESD resistance on the EL lamp outputs.

HBM ESD Protection

Figure 8a shows the Human Body Model, and Figure 8b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

Design Procedure

LX Inductor Selection

The recommended tapped-inductor ratio is 1:7 with a 2.3µH primary inductance and 115µH secondary inductance. For most applications, the primary series resistance (DCR) should be below 1Ω for reasonable efficiency. Do not exceed the inductor's saturation current. See Table 15 for a list of recommended tapped-inductors.

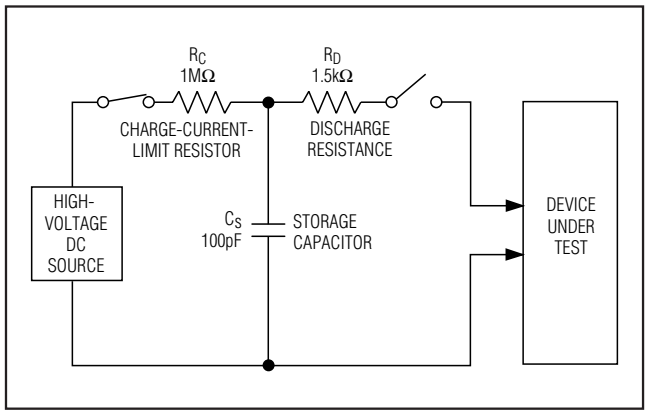

Figure 8a. Human Body ESD Test Model

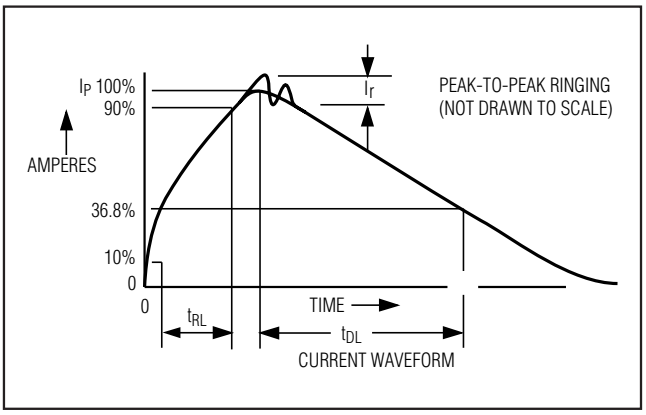

Figure 8b. Human Body Current Waveform

Table 15. Inductor Vendors

INDUCTOR VALUE (µH)	VENDOR	URL	PART NUMBER
2.3/115	Coilcraft	www.coilcraft.com	GA3250-BL
2.3/115	Cooper	www.cooper.com	CTX03-18210-R

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C_{CS} Capacitor Selection

C_{CS} is the output of the boost converter and provides the high-voltage source for the EL lamp. Connect a 3.3nF capacitor from CS to GND and place as close to the CS input as possible.

Diode Selection

Connect a diode, D1, from the LX node to CS to rectify the boost voltage on CS. The diode should be a fast recovery diode that is tolerant to +200V.

EL Lamp Selection

EL lamps have a capacitance of approximately 2.5nF to 3.5nF per square inch. See the Total Input Current vs. Load graph in the *Typical Operating Characteristics* section for compatible lamp sizes.

Snubber Selection

An R_{SN} value of 20Ω and C_{SN} value of 330pF is sufficient for V_{DD} < 5V and C_{LAMP_TOTAL} < 40nF. For higher capacitive loads on the EL output or for V_{DD} > 5V, C_{SN} must be increased to keep LX spikes less than 30V.

f_{SW} Selection

Choose a boost-converter frequency such that the saturation current of the tapped-inductor primary coil is not exceeded. Special attention must be given to program the FSW bits properly when V_{BAT} > 5.5V to avoid destruction of the device. In general, it is good practice to start from the highest f_{SW} setting (1.6MHz) and decrease accordingly to obtain the acquired waveshape on the EL outputs and to prevent exceeding the saturation current of the tapped-inductor.

Applications Information

PCB Layout

Keep PCB traces as short as possible. Ensure that bypass capacitors are as close to the device as possible. Use large ground planes where possible.

Chip Information

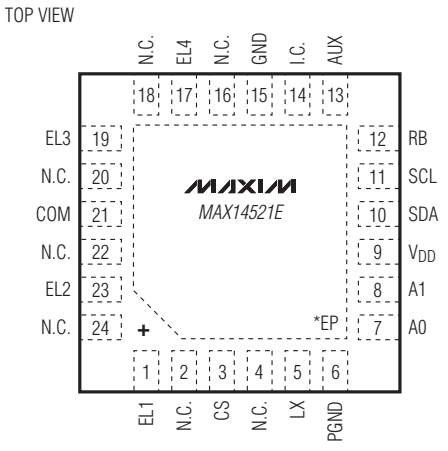
PROCESS: BiCMOS-DMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
24 TQFN-EP	T2444M-1	**21-0139**

Pin Configuration



TQFN-EP

*EXPOSED PAD. CONNECT EP TO GND.